REMARKS

Reconsideration of the patent application in view of the following remarks is respectfully requested. Applicants have amended the preamble of Claim 35 to provide antecedent basis for the later recited "integrated circuit."

Objection to the Specification

In the office action dated November 1, 2003, the Examiner objected to the specification due to the presence of redundant phrases at the end of the instant application's Detailed Description. An associate from the offices of Stattler, Johansen & Adeli LLP, Jeffrey McKinney, telephoned the Examiner on April 30, 2003 regarding the location of the allegedly redundant subject matter. The Examiner stated that the subject matter was in Claim 1, which was cancelled in a Preliminary Amendment filed concurrently with the instant application. Applicants respectfully submit that the Examiner's objection is accordingly moot.

Rejection of the Claims Under 35 U.S.C. § 102(e)

In the office action dated November 1, 2003, the Examiner rejected claims 21-35 under 35 U.S.C. § 102(e). The Examiner stated that the claimed invention was anticipated by U.S. Patent No. 6,150,193 to Glenn. Applicants respectfully traverse the Examiner's rejection.

I. Glenn Is Directed to a Shielded Package for an Integrated Circuit Chip

In U.S. Pat. No. 6,150,193, Glenn reports a shielded package for an integrated circuit chip. The package contains an "insulating substrate having metallizations formed on the surface of the substrate." [col. 2, lns 24-26] An integrated

circuit is mounted onto the package substrate surface, and circuit bonding pads are electrically coupled to the substrate metallizations. [col. 2, lns 27-28] Packaging is completed by the addition of an encapsulant layer and an electrically conductive shield layer. [col. 2, lns 29-32]

In other words, Glenn's invention concerns a package—something that encloses an integrated circuit—not an integrated circuit *per se*.

II. Figures 7-9 and 13b of Glenn Illustrate a Shielded Package for an Integrated Circuit

The Examiner specifically points to Figures 7-9 and 13b of Glenn as disclosing an integrated circuit. According to Glenn, however, the figures illustrate shielded packages, not integrated circuits:

> FIGS. 7A and 7C are top plan and bottom plan views, respectively, of a [shielded package] substrate in accordance with the present invention. [col. 3, lns 45-47]
>
> FIG. 7B is a cross-sectional view along the line VB-VB of FIG. 7A of the [shielded package] substrate. [col. 3, lns 48-49]
>
> FIGS. 8A, 8B and 8C are cross-sectional (taken along the line VIA-VIA of FIG. 7A), top plan and bottom plan views, respectively, of a region of the substrate of FIG. 7A. [col. 3, lns 50-52]
>
> FIGS. 9A and 9B are cross-sectional and top plan views, respectively, of shielded package 10B (FIG. 3) during fabrication. [col. 9, lns 9-11]
>
> FIGS. 13A and 13B are cross-sectional and bottom plan views, respectively, of shielded package 10B further along in processing. [col. 10, lns 57-59]

Applicants respectively submit that the Examiner has mistaken the substrate metallizations of Glenn's shielded packages as integrated circuit wires.

III. Applicants' Invention Is Directed to an Integrated Circuit

Applicants point with particularity to the nature of their invention in the abstract of the instant application:

> An **integrated circuit** has a metal layer that includes conductors to provide interconnectivity for components of the integrated circuit chip. The metal layer is divided into at least two sections, such that a first section has a preferred direction and the second section has a preferred wiring direction that is different from the first preferred direction. The first and second preferred directions on a single metal layer may consist of any direction. The metal layer may be divided into more than two sections, wherein each section has a preferred wiring direction. Wiring geometries for multi-level layers are also disclosed. (Emphasis added.)

The present invention is directed to an integrated circuit, not to a package containing an integrated circuit.

IV. Applicants' Independent Claims 21 and 26 Are Limited to an Integrated Circuit

Independent claims 21 and 26 of the instant application both contain the preamble, "An integrated circuit comprising . . . ." This preamble limits the structure of the claimed article, specifying that described elements must be contained within the boundaries of an integrated circuit. Described elements contained in a structure other

than an integrated circuit are not embraced by the subject claims. (See MPEP Sec. 2111.02.)

V. Applicants' Independent Claim 35 Is Limited to a Method for Simulating Wiring Direction on an Integrated Circuit

Independent claim 35 of the instant application, as amended, contains the preamble, "A method for simulating any wiring direction in an integrated circuit using wires deposed in diagonal and Manhattan directions, the method comprising the steps of . . ." Again, as for Claims 21 and 26 discussed above, this limits the method to being performed with respect to an integrated circuit; it does not embrace a method performed with respect to other structures.

VI. Glenn's Discussion of a Package Accordingly Does Not Anticipate Claims 21-35

Because the subject claims are limited to integrated circuits or methods performed with respect to integrated circuits, they do not read on any disclosure made in Glenn. Applicants therefore respectfully request that the Examiner's rejection under 35 USC Sec. 102(e) be removed.

CONCLUSION

In view of the foregoing, it is submitted that the claims are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

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Dated: 5/1/03

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The Amended Claims

The following pages provide the amended claims with the amendments marked with deleted material in [brackets] and new material underlined to show the changes made.

35. (Once Amended) A method for simulating any wiring direction in an integrated circuit using wires deposed in diagonal and Manhattan directions, the method comprising the steps of:

providing at least one metal layer comprising at least two pairs of conductors to interconnect one or more points on the integrated circuit, wherein a conductor comprises one or more wires and a wire comprises a continuous segment deposed in a single direction;

for each pair of conductors:

deposing a first wire in a Manhattan direction relative to the boundaries of the integrated circuit, the first wire comprising a first wire length including first and second ends;

deposing a second wire in a diagonal direction relative to the boundaries of the integrated circuit, the second wire comprising a second wire length including first and second ends;

coupling the first end of the second wire to the second end of the first wire; and

wherein, an effective direction of the pairs of conductors comprises an angle, A, measured relative to the boundaries of the integrated circuit, defined by the expression Tan A = Y/X,

wherein, Y comprises a line segment with a distance starting from the second end of the second wire in the last conductor pair and ending at an intersection with a line segment propagated from the first end of the first wire and in the direction of the first wire, and X comprises a distance, measured in the direction of the first wire, starting from the first end of the first wire and ending with the intersection of the Y line segment.